

# NTHS5441

## Power MOSFET

-20 V, -5.3 A, P-Channel ChipFET™

### Features

- Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 sec	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-20		V
Gate-Source Voltage	$V_{GS}$	$\pm 12$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	-5.3 -3.8	-3.9 -2.8	A
Pulsed Drain Current	$I_{DM}$	$\pm 20$		A
Continuous Source Current (Note 1)	$I_S$	-5.3	-3.9	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

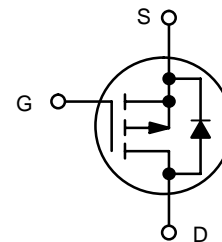
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



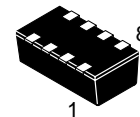
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-20 V	46 m $\Omega$ @ -4.5 V	-5.3 A

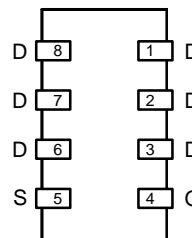


P-Channel MOSFET

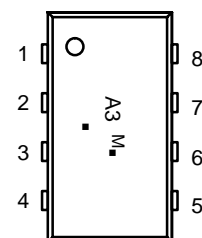


ChipFET  
CASE 1206A  
STYLE 1

### PIN CONNECTIONS



### MARKING DIAGRAM



A3 = Specific Device Code

M = Month Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTHS5441T1	ChipFET	3000/Tape & Reel
NTHS5441T1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHS5441

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2) t ≤ 5 sec Steady State	R <sub>θJA</sub>	40 80	50 95	°C/W
Maximum Junction-to-Foot (Drain) Steady State	R <sub>θJF</sub>	15	20	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.6		-1.2	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1.0	μA
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85°C			-5.0	
On-State Drain Current (Note 3)	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5.0 V, V <sub>GS</sub> = -4.5 V	-20			A
Drain-Source On-State Resistance (Note 3)	r <sub>DS(on)</sub>	V <sub>GS</sub> = -3.6 V, I <sub>D</sub> = -3.7 A V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A	-	0.050 0.046	0.06 -	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -3.1 A		0.070	0.083	
Forward Transconductance (Note 3)	g <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -3.9 A		12		mhos
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	I <sub>S</sub> = -2.1 A, V <sub>GS</sub> = 0 V		-0.8	-1.2	V

## Dynamic (Note 4)

Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.9 A		9.7	22	nC
Gate-Source Charge	Q <sub>GS</sub>			1.2		
Gate-Drain Charge	Q <sub>GD</sub>			3.6		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -5.0 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz		710		pF
Output Capacitance	C <sub>oss</sub>			400		
Reverse Transfer Capacitance	C <sub>rss</sub>			140		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ -1.0 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω		14	30	ns
Rise Time	t <sub>r</sub>			22	55	
Turn-Off Delay Time	t <sub>d(off)</sub>			42	100	
Fall Time	t <sub>f</sub>			35	70	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.1 A, di/dt = 100 A/μs		30	60	

2. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

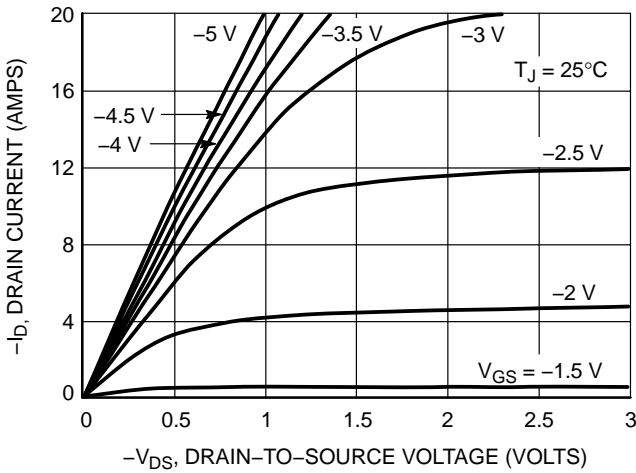


Figure 1. On-Region Characteristics

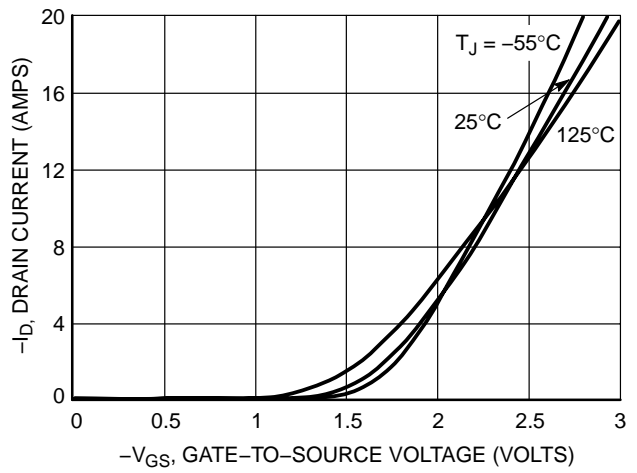


Figure 2. Transfer Characteristics

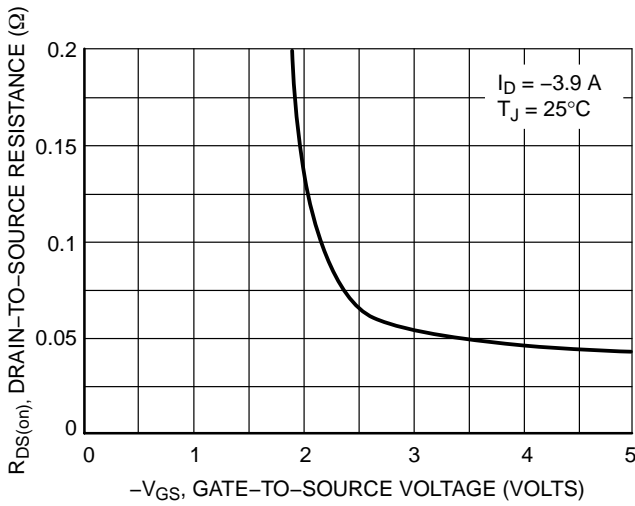


Figure 3. On-Resistance versus Gate-to-Source Voltage

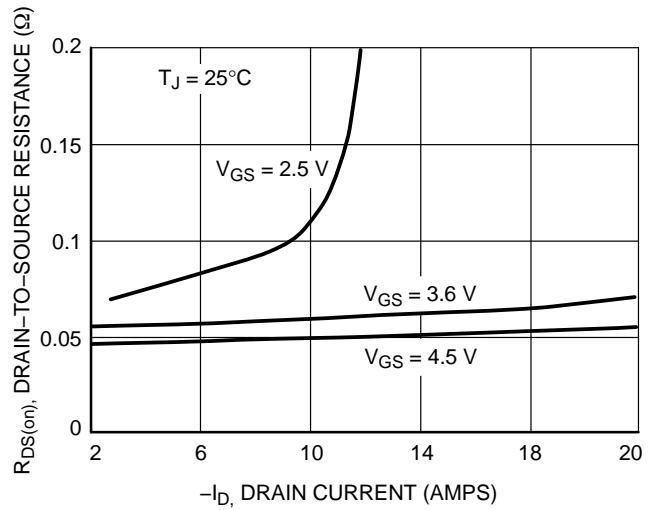


Figure 4. On-Resistance versus Drain Current and Gate Voltage

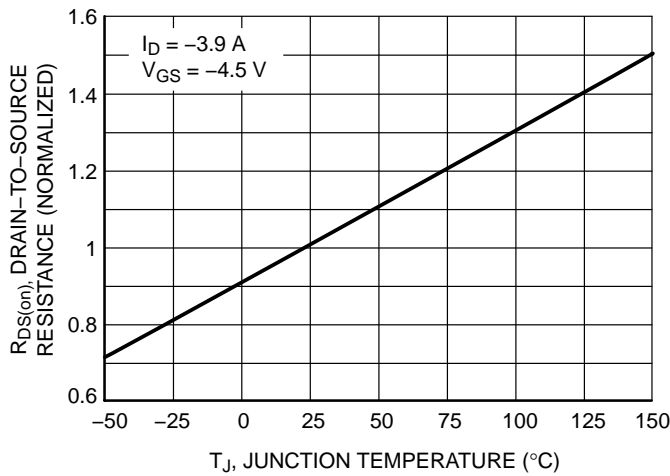


Figure 5. On-Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

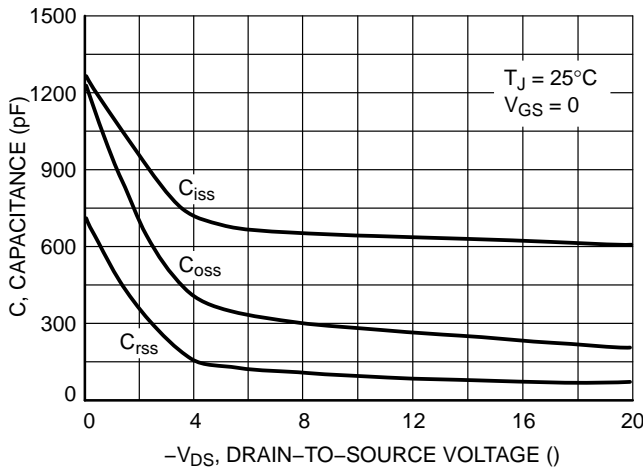


Figure 6. Capacitance Variation

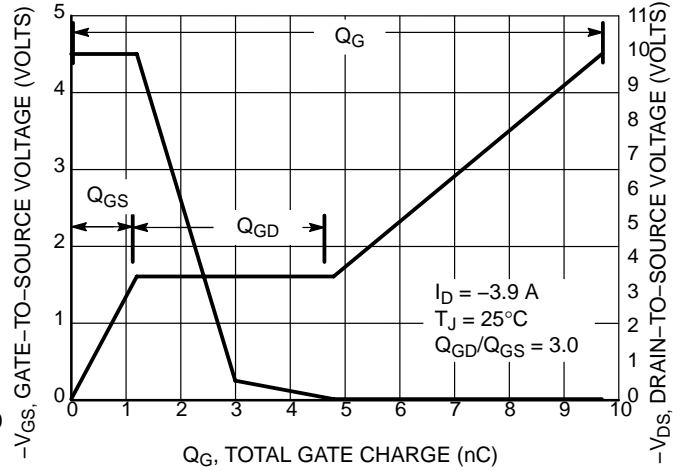


Figure 7. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

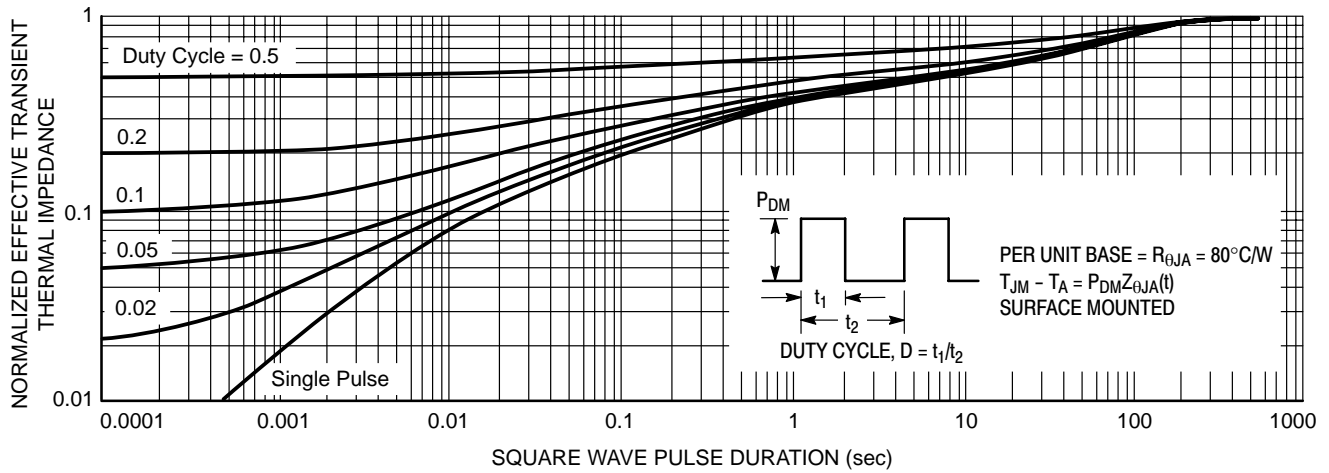


Figure 8. Normalized Thermal Transient Impedance, Junction-to-Ambient

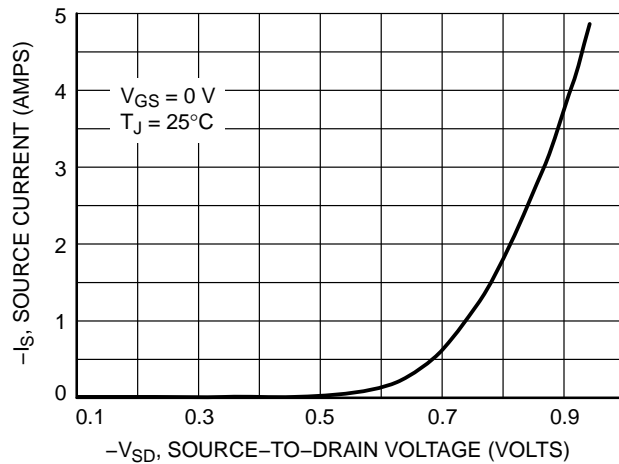
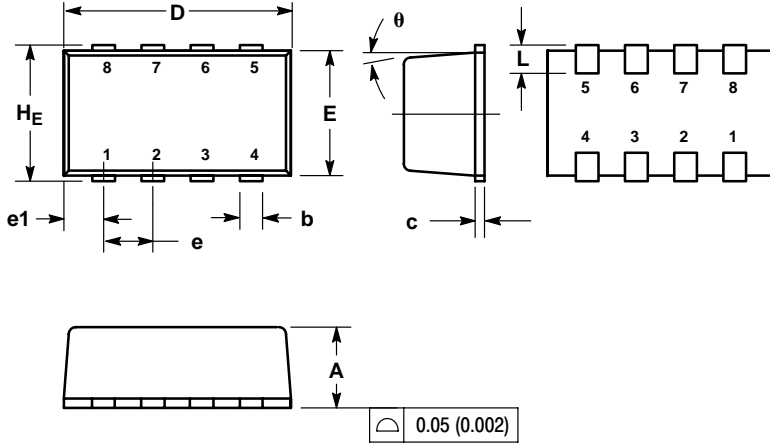


Figure 9. Diode Forward Voltage versus Current

# NTHS5441

## PACKAGE DIMENSIONS

### ChipFET™ CASE 1206A-03 ISSUE G

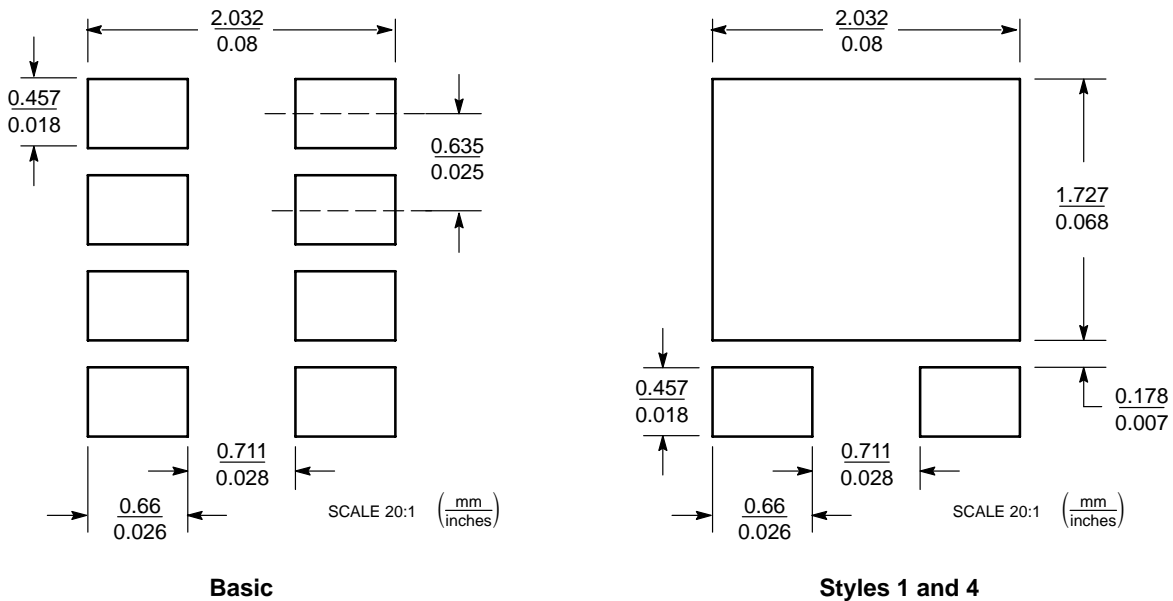


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.


DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
HE	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ChipFET is a trademark of Vishay Siliconix.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your  
local Sales Representative.